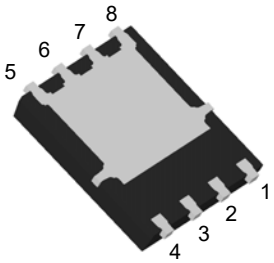
NA7350D

N-Channel 30-V (D-S) MOSFET



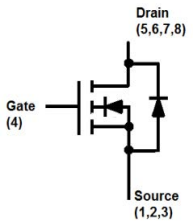
DFN5060-8B

1. FEATURES

- Low RDS(on) trench technology.
- Fast switching speed.
- Low thermal impedance.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

2. APPLICATIONS

- White LED boost converters
- Automotive Systems
- Industrial DC/DC Conversion Circuits



3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
NA7350D	LN7350	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits	Unit
Drain−to−Source Voltage		VDS	30	V
Gate−to−Source Voltage		VGS	±20	V
Continuous Drain Current(Note 1)	TA =25°C	ID	40	A
	TA =70°C		32	
Pulsed Drain Current (Note 2)		IDM	100	
Continuous Source Current (Note 1) (TA =25°C,VGS=0V)		IS	7	A
Pulsed Source Current (Note 2) (TA=25°C,Tp=8/20us)		ISM	121	A
Avalanche Current (L = 0.1mH)		IAS	21	A
Avalanche Energy (L = 0.1mH)		EAS	22	mJ
Power Dissipation(Note 1)	TA =25°C	PD	5	W
	TA =70°C		3.2	
	TC=25°C		50	
Operating Junction Temperature		TJ	−55 ~+150	℃
Storage Temperature Range		Tstg	−55 ~+150	

1.Surface Mounted on 1” x 1” FR4 Board.

2.Pulse width limited by maximum junction temperature.

5. THERMAL CHARACTERISTICS

Parameter		Symbol	Max	Unit
Maximum Junction-to-Ambient(Note 1)	t≤ 10s	RθJA	25	℃/W
	Steady-State		65	
Maximum Junction-to-Case		RθJC	2.5	℃/W

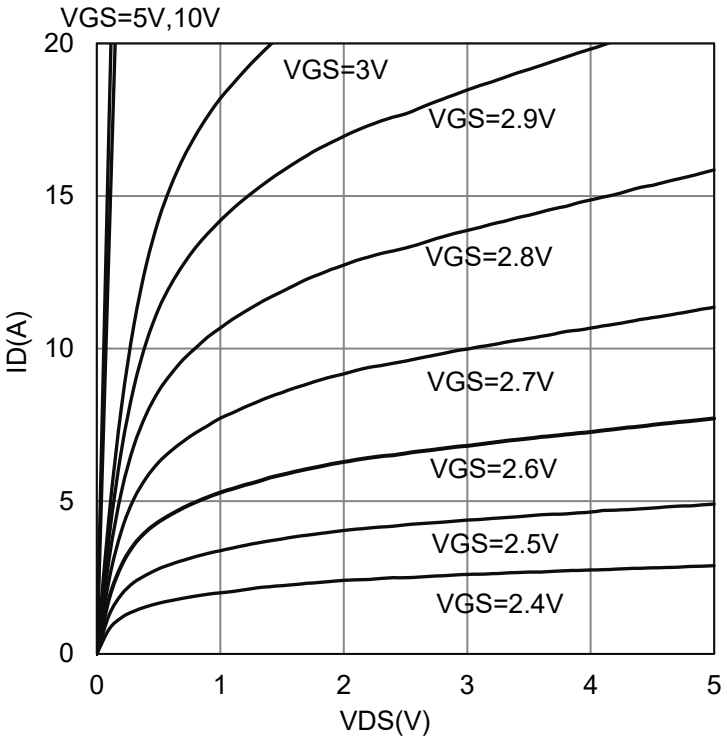
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage (VDS = VGS , ID = 250 uA)		VGS(th)	1	-	3	V
Gate-Body leakage current (VDS =0V, VGS = ±20V)		IGSS	-	-	±10	uA
Zero Gate Voltage Drain Current (VDS = 24 V, VGS = 0 V) (VDS = 24 V, VGS = 0 V, TJ = 55°C)		IDSS	- -	- -	1 25	μA
Drain-to-Source On-Resistance (VGS = 10 V, ID = 15 A) (VGS = 4.5 V, ID = 12 A)		RDS(ON)	- -	5.5 7.2	6.5 9	mΩ
Diode Forward Voltage (IS = 3.2 A, VGS = 0 V)		VSD	-	0.79	1.2	V
Dynamic						
Total Gate Charge	(VDS = 15 V, VGS = 4.5 V,ID = 15 A)	Qg	-	15.7	-	nC
Gate to Source Charge		Qgs	-	4.7	-	
Gate to Drain Charge		Qgd	-	6	-	
Turn-on Delay Time	(VDD=15 V,RL =1Ω,ID=15 A,VGEN=10 V RGEN = 6 Ω)	td(on)	-	6	-	nS
Rise Time		tr	-	6	-	
Turn-Off Delay Time		td(off)	-	28	-	
Fall Time		tf	-	8	-	
Input Capacitance	(VDS = 15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	1561	-	pF
Output Capacitance		Coss	-	183	-	
Reverse Transfer Capacitance		Crss	-	167	-	
Gate-Resistance (VGS = 0 V, VDS=0V,f=1MHz)		Rg	-	0.84	-	Ω

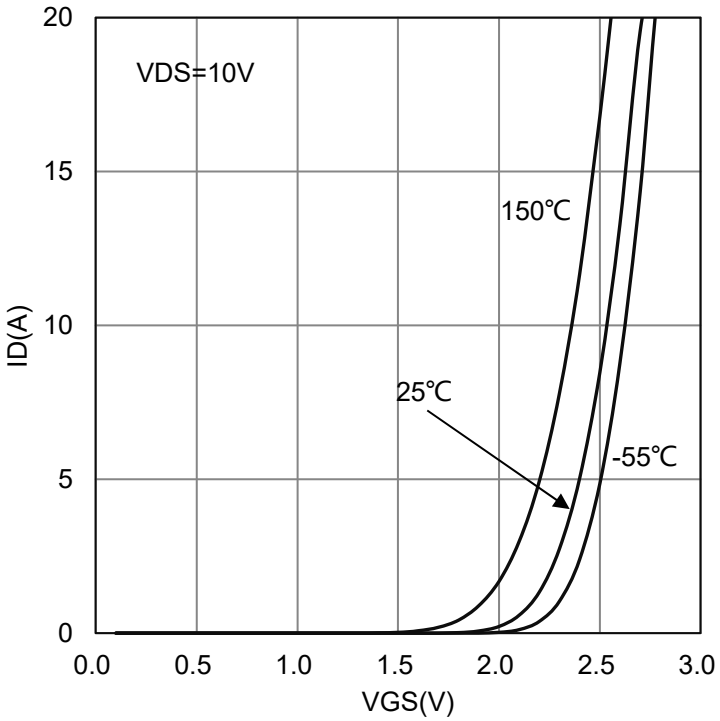
3.Pulse test: PW ≤ 300μs duty cycle ≤ 2%.

4.Guaranteed by design, not subject to production testing.

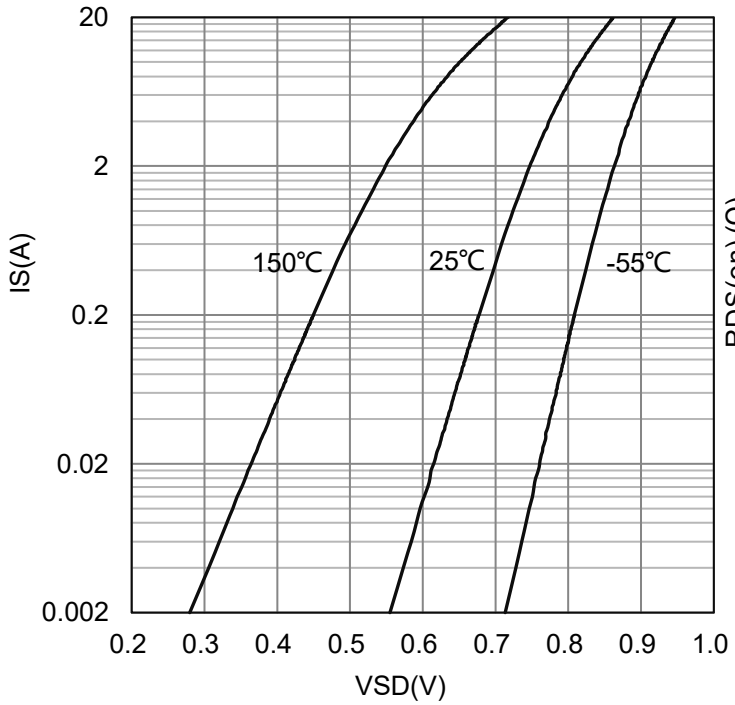
7.ELECTRICAL CHARACTERISTICS CURVES



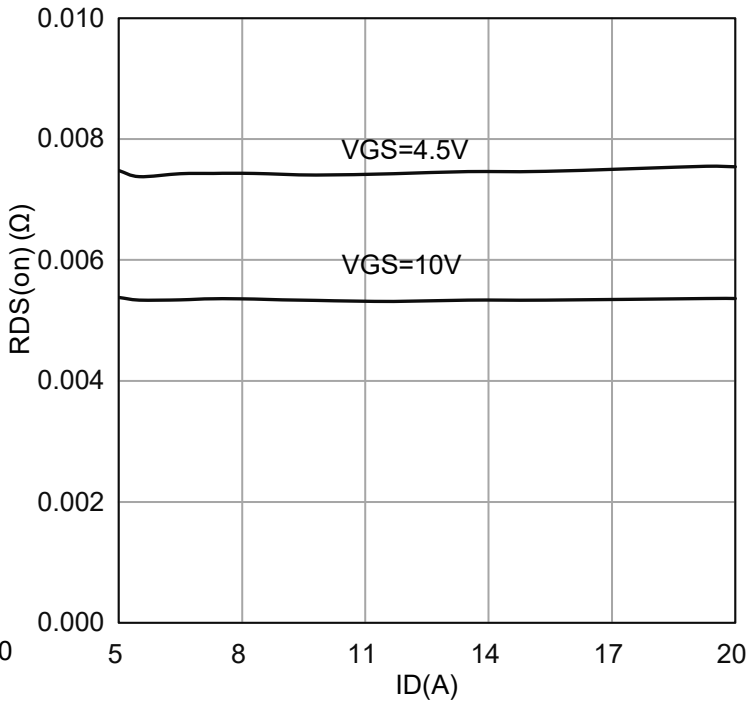
ID vs. VDS



ID vs. VGS

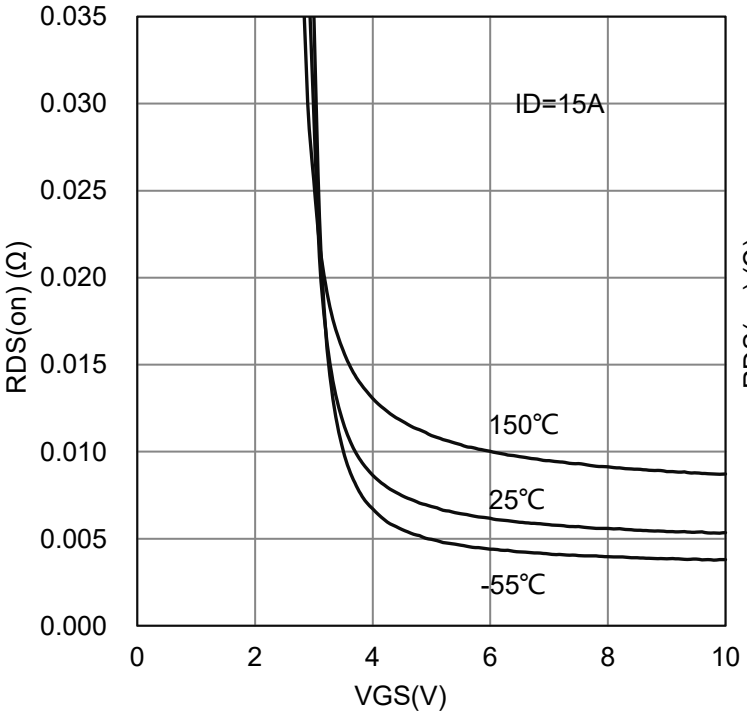


IS vs. VSD

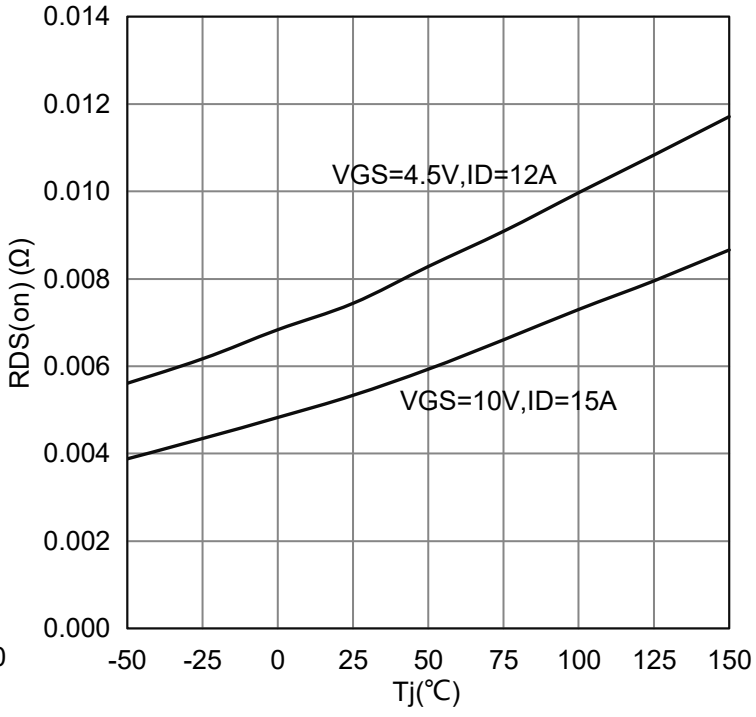


RDS(on) vs. ID

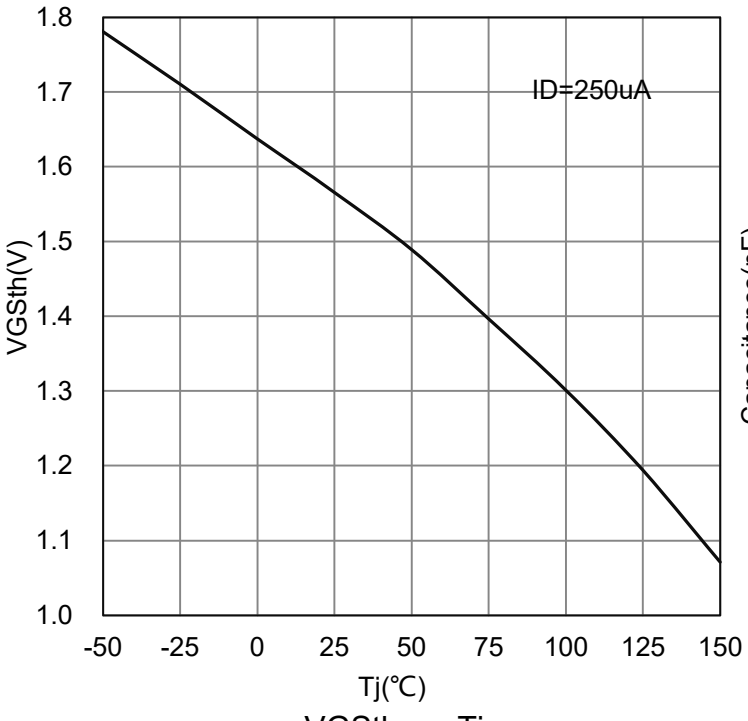
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



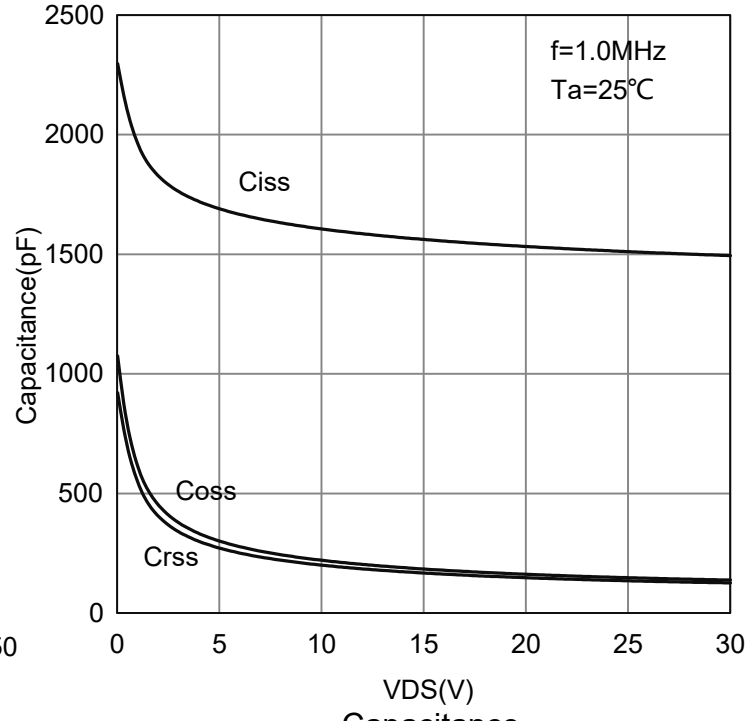
RDS(on) vs. VGS



RDS(on) vs. Tj



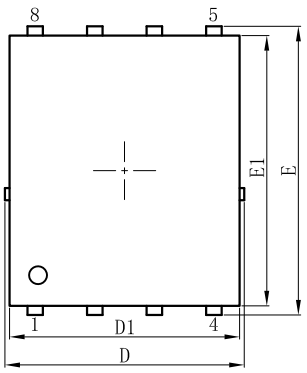
VGSth vs. Tj



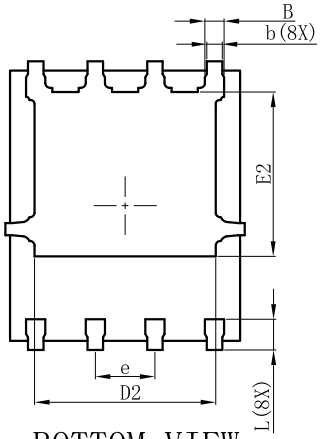
Capacitance

8.OUTLINE AND DIMENSIONS

DFN5060-8B

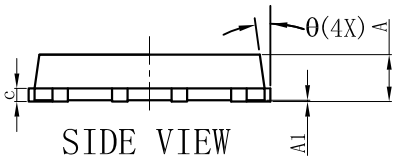


TOP VIEW



BOTTOM VIEW

DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

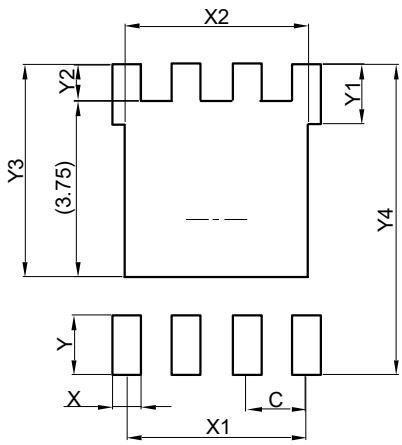


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9. SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61