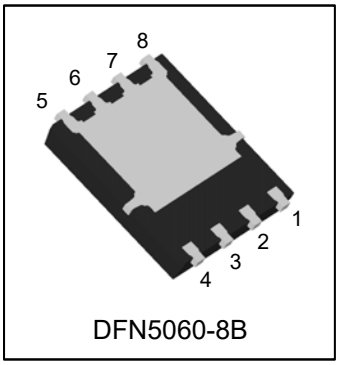
N7314D

N-Channel Logic Level Enhancement Mode MOSFET



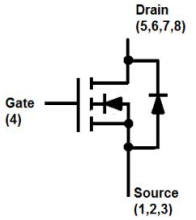
DFN5060-8B

1. FEATURES

- Low RDS(on) trench technology.
- Low thermal impedance.
- Fast switching speed.
- We declare that the material of product are Halogen Free and compliance with RoHS requirements.

2. APPLICATION

- Power Routing
- DC/DC Conversion
- Motor Drives



3. ORDERING INFORMATION

Device	Marking	Shipping
N7314D	LN7314	3000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits	Unit
Drain−to−Source Voltage		VDSS	30	V
Gate−to−Source Voltage		VGS	±20	V
Continuous Drain Current	TC =25°C	ID	20	A
	TA =25°C		13	
	TC =100°C		15	
Pulsed Drain Current (Note 1)		IDM	80	
Avalanche Current (L=0.1mH,Rg=25Ω)		IAS	18	A
Avalanche energy (L=0.1mH,Rg=25Ω)		EAS	16.2	mJ
Power Dissipation	TC =25°C	PD	35	W
	TC =70°C		22	
Operating Junction Temperature		TJ	−55 ~+150	℃
Storage Temperature Range		Tstg	−55 ~+150	

1.Pulse width limited by maximum junction temperature.

5. THERMAL CHARACTERISTICS

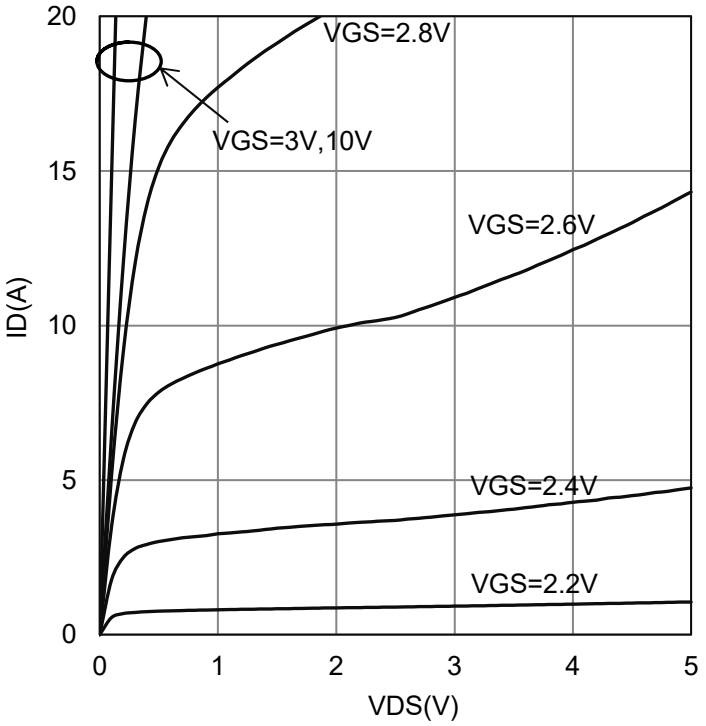
Parameter		Symbol	Limits	Unit
Maximum Junction-to-Ambient	t≤10s	RθJA	25	℃/W
	Steady State		65	
Maximum Junction-to-Case		RθJC	3.5	℃/W

6. ELECTRICAL CHARACTERISTICS(Ta = 25ºC)

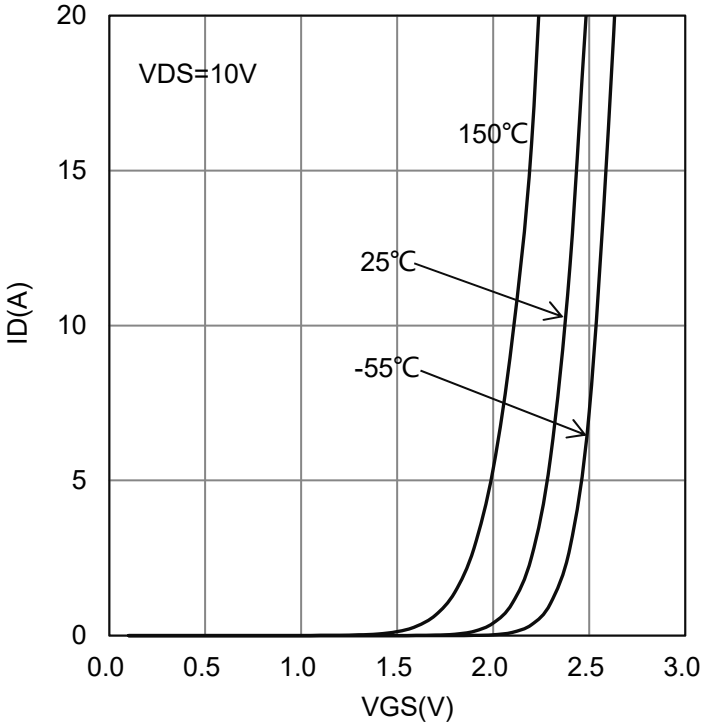
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage (VGS = 0V, ID = 250μA)		V(BR)DSS	30	-	-	V
Gate-Source Threshold Voltage (VDS = VGS , ID = 250 uA)		VGS(th)	1	1.5	3	V
Gate-Body Leakage (VDS = 0 V, VGS = ±20 V)		IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VDS = 24 V, VGS = 0 V) (VDS = 20 V, VGS = 0 V, TJ = 125°C)		IDSS	- -	- -	1 25	μA
Drain-Source On-Resistance(Note 2) (VGS = 10 V, ID = 12 A) (VGS = 4.5 V, ID = 8 A)		RDS(on)	- -	7.5 10	9 13.5	mΩ
Diode Forward Voltage(Note 2) (IF = 12 A, VGS = 0 V)		VSD	-	-	1.2	V
Dynamic						
Total Gate Charge(VGS=10V)	(VDS = 15 V, VGS = 10 V,ID = 12 A)	Qg	-	17.4	-	nC
Total Gate Charge(VGS=4.5V)		Qg	-	8.3	-	
Gate-Source Charge		Qgs	-	2.3	-	
Gate-Drain Charge		Qgd	-	3	-	
Input Capacitance	(VDS = 15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	960	-	pF
Output Capacitance		Coss	-	125	-	
Reverse Transfer Capacitance		Crss	-	85	-	
Turn-On Delay Time	(VDS = 15 V, ID=1A, VGS= 10V, RGS = 6Ω)	td(on)	-	8	-	ns
Rise Time		tr	-	15	-	
Turn-Off Delay Time		td(off)	-	20	-	
Fall Time		tf	-	20	-	
Gate-Resistance (VDS=0V,VGS=0V,f=1.0MHz)		Rg	-	3	-	Ω

2.Pulse test: PW≤ 300μs duty cycle ≤ 2%.

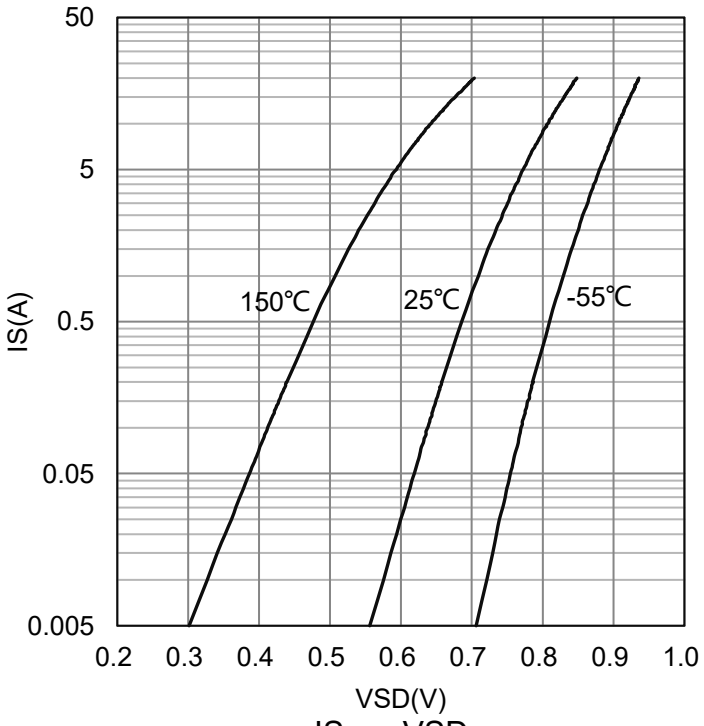
7.ELECTRICAL CHARACTERISTICS CURVES



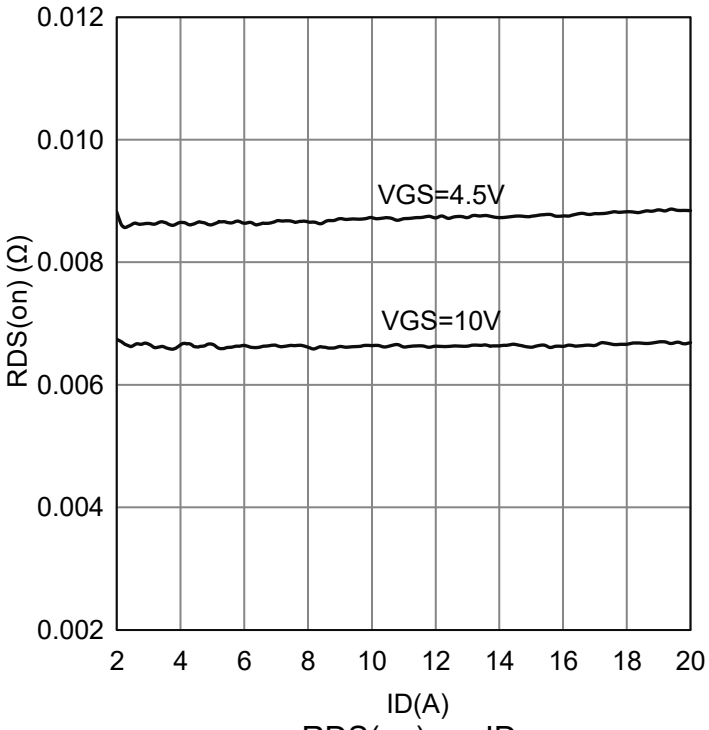
ID vs. VDS



ID vs. VGS

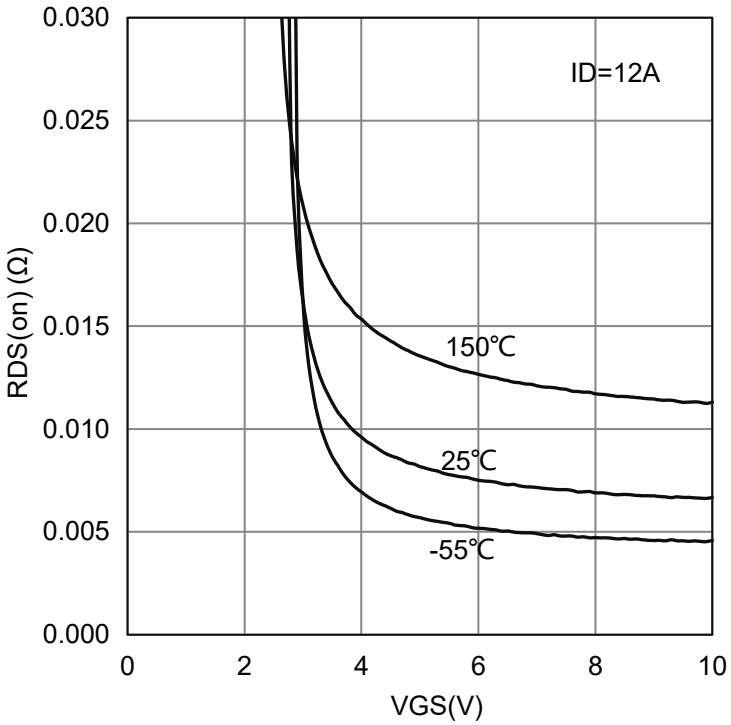


IS vs. VSD

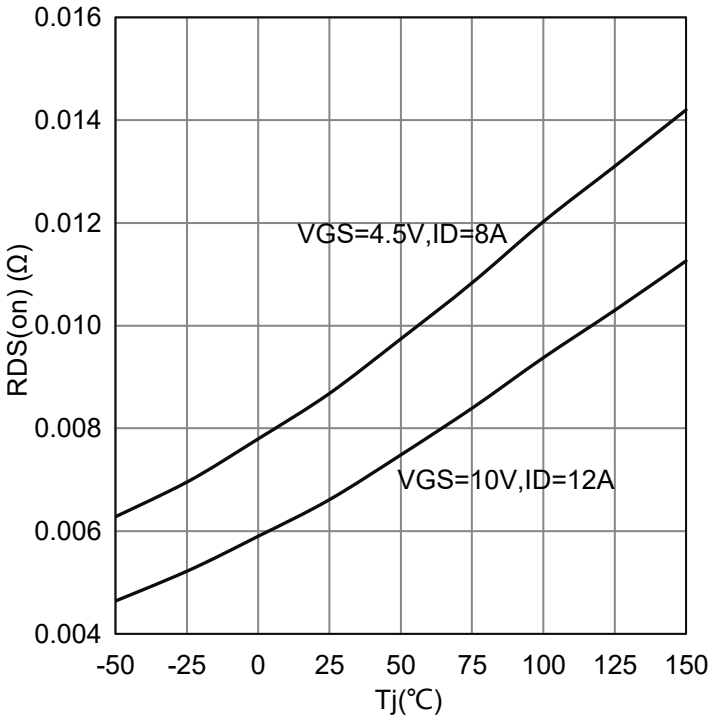


RDS(on) vs. ID

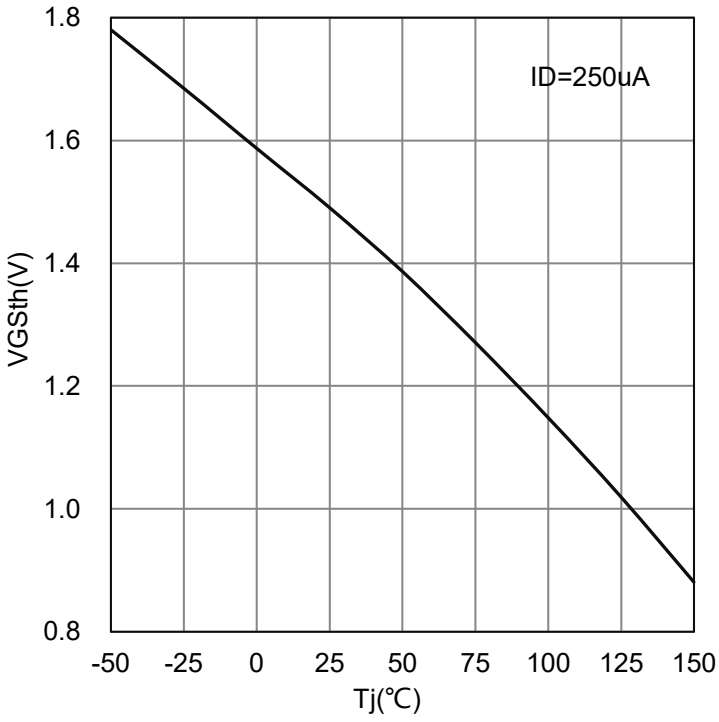
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



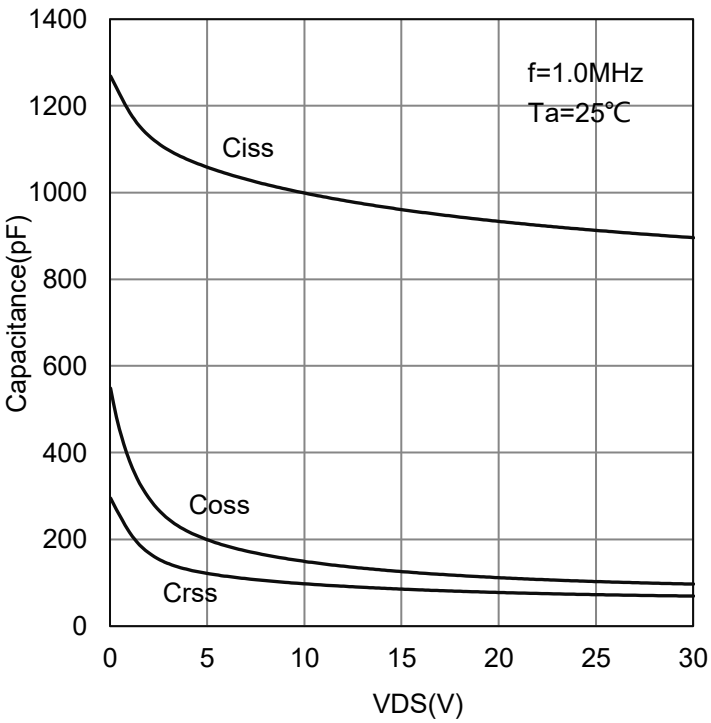
RDS(on) vs. VGS



RDS(on) vs. Tj



VGSth vs. Tj



Capacitance

8.OUTLINE AND DIMENSIONS

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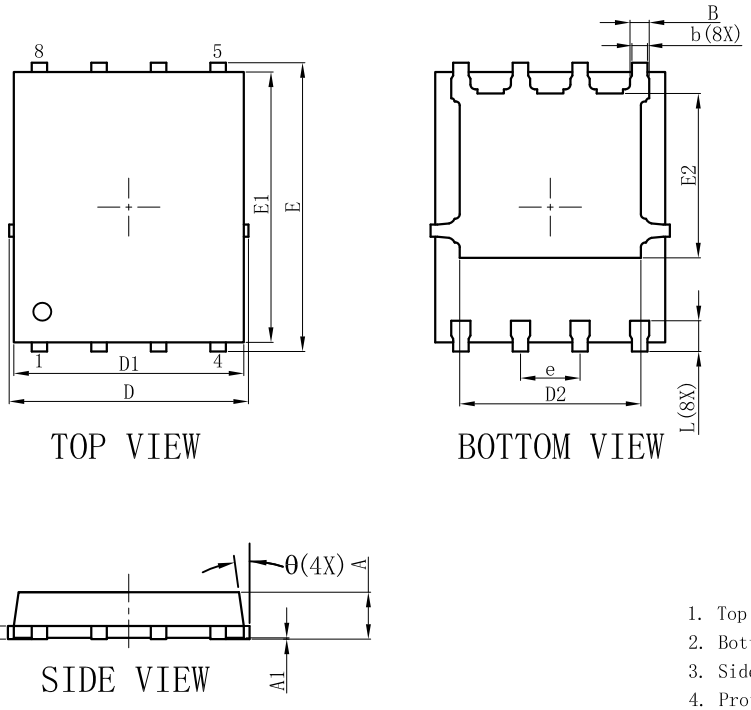
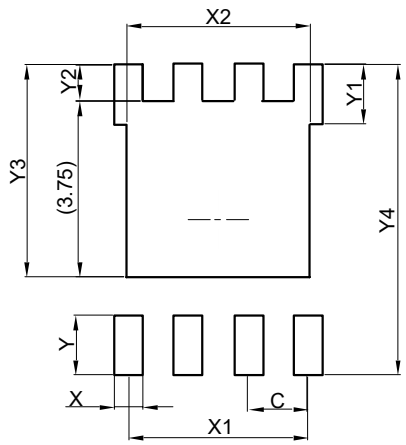


DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61